What is claimed is:

1. A semiconductor memory device comprising a memory cell array in which a plurality of static type memory cells comprised of driver MOSFET, transfer MOSFET and load devices are arranged, the semiconductor memory device comprising:

a switch for controlling a source line connected to a source electrode of said driver MOSFET and a ground potential line so that the lines are connected in an operational state of said memory cells and the lines are not connected in a standby state of said memory cells; and

a source potential control circuit connected between said source line and said ground potential;

wherein, in the standby state of said memory cells, a source potential is set to an intermediate potential between the ground potential and the supply potential by said source potential control circuit.

2. A semiconductor memory device according to claim 1, wherein said source potential control circuit is comprised of an n-channel MOSFET in which a drain electrode and a gate electrode are connected to said source line and the source electrode is connected to said ground potential line.

3. A semiconductor memory device according to claim

1, wherein said source potential control circuit is comprised of: an n-channel MOSFET in which a drain electrode and a gate electrode are connected to said source line and the source electrode is connected to said ground potential line; and a resistance that connects between said source line and said ground potential line.

4. A semiconductor memory device according to claim 3, wherein said resistance is comprised of an n-channel MOSFET in which a drain electrode is connected to said source line, a source electrode is connected to said ground potential line, and a gate electrode is connected to said supply potential line.

5. A semiconductor memory device according to claim 1, wherein said switch is a switch MOS that is comprised of an n-channel MOSFET in which a drain electrode, a source electrode and a gate electrode are connected to said source line, said ground potential line, and a control signal line for controlling said switch, respectively.

6. A semiconductor memory device according to claim 5, wherein said switch MOS is disposed between said memory cell array and a sense amplifier that operates when data is read out.

7. A semiconductor memory device according to claim 1, comprising: said memory cell array; an access circuit for accessing said memory cells; and a switch that is

connected between an operational potential point and a supply potential line of said access circuit.

8. A semiconductor memory device according to claim 7, wherein said access circuit comprises:

a word driver for driving a word line;

a first switch disposed between a high operational potential point of said word driver and the supply potential line; and

a second switch disposed between a low operational potential point of circuits accessing said memory cells except the word driver and the supply potential line.

9. A semiconductor memory device comprising a memory circuit in which static type memory cells are provided at an intersection point of a word line and a bit line and arranged in an array-like manner, wherein

said memory cells are comprised of driver MOSFET, transfer MOSFET and load MOSFET;

the semiconductor memory device has a source potential control circuit for controlling a potential of a source line connected to a source electrode of said driver MOSFET; and

a negative voltage is applied to the word line connected to the memory cells that are not selected in the operational state of said memory circuit and the word line is set to a ground potential in the standby state of said

memory circuit.

10. A semiconductor memory device according to claim 9, wherein, when data is read out from said memory circuit, said source potential is set to the ground potential and, when the data is written to said memory circuit or in the standby state, said source line potential is set to an intermediate potential between the ground potential and a supply potential by said source potential control circuit.

11. A semiconductor memory device according to claim 9, wherein a drain electrode of said transfer MOSFET is connected to the bit line and, when said source line is set to an intermediate potential between the ground potential and the supply potential, the potential of said bit line is set to the supply potential.

12. A semiconductor memory device according to claim 9, wherein a threshold voltage of said driver MOSFET is higher than a threshold voltage of said transfer MOSFET.

13. A semiconductor memory device according to claim 9, wherein an absolute value of the threshold voltages of said transfer MOSFET and said driver MOSFET is lower than an absolute value of a threshold voltage of said load MOSFET.

14. A semiconductor memory device according to claim 9, wherein a logic circuit including a first MOSFET having a first threshold voltage and a second MOSFET having a

second threshold voltage higher than said first threshold voltage is packaged together on a substrate on which said memory circuit is disposed, and wherein said first MOSFET is used as said transfer MOSFET and said second MOSFET is used as said driver MOSFET.

15. A semiconductor memory device comprising a memory array in which static type memory cells comprised of a pair of driver MOSFET, a pair of transfer MOSFET and a pair of load devices are arranged in an array-like manner, wherein

a first area in which said memory cells are arranged in a direction perpendicular to the bit line at one end of said memory array is provided, a portion of a gate layer of the MOSFET disposed in said first area is connected to a ground potential and the other portion of said gate layer is connected to a signal line for controlling an operational potential of the memory cells.

16. A semiconductor memory device according to claim 15, wherein, in a layout pattern of said memory cells, said pair of driver MOSFET, said pair of transfer MOSFET and said pair of load devices are arranged symmetrically with respect to a predetermined point in the pattern of said memory cells.

17. A semiconductor memory device according to claim 15, wherein a portion of MOSFET formed in said first area

is used for the switch according to claim 1.